RAMAKRISHNA MISSION VIDYAMANDIRA

(Residential Autonomous College affiliated to University of Calcutta)

B.A./B.Sc. SIXTH SEMESTER EXAMINATION, MAY 2025

THIRD YEAR [BATCH 2022-25]

Date : 07/05/2025 **PHYSICS (HONOURS)**

Time : 11 am – 1 pm **Paper : CC 14** Full Marks : 50

Answer **any five** questions: [5×10]

1. a) Draw the voltage transfer characteristics of a transistor as a switch and explain in which regions the switch is operated.
   b) Define the Figure of Merit and Fan out of an IC.
   c) Explain the purpose of the totem-pole output stage used in a TTL gate.
   d) Design a CMOS NAND gate and verify the truth table. [2+2+3+3]

2. a) A number is in 2's complement representation is (10010). Find its decimal equivalent of said number.
   b) Find the binary number of the gray code 111011. Write an application of gray code in digital circuit.
   c) What is Shannon's Expansion Theorem? Prove the following using this theorem
   $A.[AB + \overline{A}D + (A + C).(\overline{A} + E) = A.(B + E)$
   d) Convert $(EABC)_{16}$ to $(?)_{10}$ and $(10111.1011)_2$ to $(?)_{10}$ [2+2+3+3]

3. a) Prove the DeMorgan's Theorem using basic postulates of Switching Algebra.
   b) Convert the following Boolean expression to equivalent canonical SOP form
   $$F(X,Y,Z) = X.\overline{Y} + Y.\overline{Z}$$
   c) What are the conditions to be a function self-dual? Find the probable number in place of '?' to the self-dual function $f(A,B,C) = \sum m(1,2,4,?)$.
   d) Minimize the Boolean expression using k-map
   $$f(A,B,C) = \sum m(2,3,4,5) + \sum d(1,7)$$
   $$f(A,B,C) = \sum m(0,1,6,7) + \sum d(3,4,5)$$ [2+2+3+3]

4. a) What is the minimum number gates required to implement the Boolean function $(AB + C)$ if we have to use only 2-input NOR gates?
   b) Implement the function $f(A,B,C) = \sum m(0,2,3,4,6,7)$ using one 4×1 MUX.
   c) Design a full adder using 4 × 1 MUX, considering AB as select line.
   d) What types of Decoders are used to convert binary to octal and binary to hexadecimal number?
   [2+4+2+2]

5. a) What is Race-around condition?
   b) Design a J-K flip-flop using S-R flip-flop with the help of excitation table.
   c) In SISO and PISO, how many clocks are required to store and output n-bit data.
   d) Design a Mod-8 up counter using +ve edge trigger clock pulse. [2+4+2+2]

6. a) Show that the total power for a fully amplitude modulated wave is 1.5 times the unmodulated carrier power. For this case, draw the relative amplitude plot in frequency domain.
   b) Calculate the power developed by an AM wave in a load of 50 Ω when the peak voltage of the carrier is 100 volt and the modulation index is 0.6.
   c) What is VCO? State its working principle. [(2+1)+3+(1+3)]

7. a) "PM modulation and demodulation can be obtained through FM modulator and demodulator respectively" – explain how this can be done.
   b) Explain the process of pulse code modulation (PCM). Describe its major components.
   c) A message signal represented by the equation $v(t) = sin^2(1000\pi t) - cos^2(500\pi t)$ is converted into PCM. Determine the minimum sampling rate for the process. [3+(3+2)+2]

8. a) What do you mean by QAM? Describe the process of generation of M-ary QAM.
   b) Compare the advantages and disadvantages of ASK, FSK and PSK.
   c) In a PCM system a 5-bit encoder is used. In this PCM system each level is represented by integer multiples of 1 volt. An analog sample of 25.86 volt is required to be digitized. Find the digital output and also determine the value of quantization error. [(1+3)+3+3]

———— × ————